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EXAMINER	
KROFCHECK, MICHAEL C	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/713,563	ELLIS, ROBERT M.	
	Examiner	Art Unit	
	Michael Krofcheck	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 April 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17 and 22-27* is/are pending in the application.

4a) Of the above claim(s) *16,17 and 22-24* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15 and 25-27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 October 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to the RCE filed on 4/12/2007.

2. Claims 1, 2, 5, 14, 25 have been amended.

3. Claim 28 has been cancelled.

4. The objections/rejections from the prior correspondence not restated herein have been withdrawn.

Claim Rejections - 35 USC § 112

5. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

6. Claim 27 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Claim 27 indicates that, "the corresponding data lane is a serial data lane." However, upon examination of the figures and specification the examiner cannot find any reference that explicitly indicates the data lane as a serial data lane. The applicant is invited to specifically point out what portion of the application is being relied upon for support of this.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

9. Claims 1-5, 7, and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Halbert et al., US patent application publication 2002/0112119, Kim, US patent application publication 2003/0174544, and Wong et al., US patent 5239561.

10. With respect to claim 1, Halbert teaches of a point-to-point memory channel having a plurality of data lanes (fig. 10-13; paragraph 0053-0056; Shown in figures 10 and 12, the paths contain multiple lanes).

Halbert fails to explicitly teach of calculating an achieved data transition density for at least one data lane in a memory channel having a plurality of data lanes, the achieved data transition density calculated over greater than two clock cycles; and

transmitting a synchronization signal on the at least one data lane responsive to the achieved transition density.

However, Kim teaches of a method comprising calculating an achieved data transition density for at least one data lane in a memory channel having a plurality of data lanes (paragraph 0018-0022); and

transmitting a synchronization signal on the at least one data lane responsive to the achieved transition density (paragraph 0020, 0023-0025).

Wong teaches of the achieved data transition density being calculated over greater than two clock cycles (abstract, column 2, lines 16-33, column 8, lines 49-52).

It would have been obvious to one of ordinary skill in the art having the teachings of Halbert, Kim at the time of the invention to include the output driver of Kim in the DIMM memories of Halbert. Their motivation would have been to improve the timing margin of a memory operation (Kim, paragraph 0009).

It would have been obvious to one of ordinary skill in the art having the teachings of Halbert and Kim and Wong at the time of the invention to determine the transition density over any number of clock cycles in the combination of Halbert and Kim as taught in Wong. Their motivation would have been to ensure DCD/DDJ compliance (column 1, lines 26-33).

11. With respect to claim 2, Kim teaches of wherein calculating an achieved data transition density for the at least one data lane comprises: counting how many times a data transition occurs on the at least one data lane during a predetermined number of clock cycles (paragraph 0019-0020).

Wong teaches of the predetermined number of clock cycles being greater than two (abstract, column 2, lines 16-33, column 8, lines 49-52).

12. With respect to claim 3, Kim teaches of storing a desired data transition density for the at least one data lane (paragraph 0020-0022; as the value of N/2 is used as the threshold, it is abundantly clear to one of ordinary skill in the art that the N/2 value is stored in order for it to be used in the comparison); and

comparing the achieved data transition density to the desired data transition density (paragraph 0020-0022).

13. With respect to claim 4, Kim teaches of wherein transmitting a synchronization signal on the at least one data lane responsive to the achieved transition density comprises: transmitting a synchronization signal on all the data lanes if the achieved data transition density is less then the desired data transition density on the at least one data lane (paragraph 0020-0025; as the data selecting part modifies the outputting of all the data (each line) in synchronism with the new clock signals created from the control signal).

14. With respect to claim 25, Kim teaches of wherein transmitting the synchronization signal on the at least one data lane comprises: transmitting the synchronization signal having a number of transition to cause the achieved data transition density for the at least one data lane is greater than or equal to a desired data transition density (paragraph 0020, 0023-0024).

15. With respect to claim 5, Halbert teaches of a memory channel comprising: a host and a plurality of DIMMs connected in a point-to-point fashion (fig. 10-13; paragraph 0054-0055),

wherein the host includes a processor (paragraph 0004);

an outbound data channel and an inbound data channel, each having a plurality of data lanes (fig. 10-13; paragraphs 0053-0056, 0058; where an embodiment can be constructed using two data paths (channels) with unidirectional components; thus creating an outbound and an inbound path. Shown in figures 10 and 12, the paths contain multiple lanes);

Kim teaches of at least one transition detection circuit configured to detect whether an achieved data transition density on at least one data lane is less than a desired data transition density for the at least one data lane (fig. 1; item 104; paragraph 0018-0022).

Wong teaches of wherein the achieved transition density is measured over greater than two clock cycles (abstract, column 2, lines 16-33, column 8, lines 49-52).

It would have been obvious to one of ordinary skill in the art having the teachings of Halbert and Kim at the time of the invention to include the output driver of Kim in the DIMM memories of Halbert. Their motivation would have been to improve the timing margin of a memory operation (Kim, paragraph 0009).

It would have been obvious to one of ordinary skill in the art having the teachings of Halbert and Kim and Wong at the time of the invention to determine the transition density over any number of clock cycles in the combination of Halbert and Kim as

taught in Wong. Their motivation would have been to ensure DCD/DDJ compliance (column 1, lines 26-33).

16. With respect to claim 7, Kim teaches of wherein the at least one transition detection circuit is located on a corresponding one of the plurality of DIMMs (paragraph 0017, 0019; as the output driver outputs the data from the memory, it is abundantly clear to one of ordinary skill in the art that it is located as a part of the memory. In the combination of Halbert and Kim this would be on each of the DIMMs as they are separately removable memory packages).

17. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Halbert and Kim and Wong as applied to claim 5 above, and further in view of Little et al., US patent 6038655.

18. With respect to claim 6, the combination of Halbert and Kim and Wong fails to explicitly teach of a host. However, Little teaches of an output driver located on a host (abstract).

The combination of Halbert, Kim, and Little teaches of wherein the at least one transition detection circuit is located on the host (where an output driver of Kim is a part of the Halbert host).

It would have been obvious to one of ordinary skill in the art having the teachings of Halbert, Kim and Wong and Little at the time of the invention to include a data output driver of Kim in the CPU of Halbert, which is supported by Little. Their motivation would have been to reduce the skew of the output of data (Kim, paragraph 0009).

19. Claims 8-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Halbert and Kim and Wong as applied to claim 5 above, and further in view of Boggs, et al., US patent 5530696.

20. With respect to claim 8, Kim teaches of wherein the at least one transition detection circuit comprises: a plurality of data transition detectors, each configured to detect a data transition on a corresponding data lane (fig. 1; paragraph 0020; as the controller compares the inputted data on the data lines, with data previously imputed to determine a transition for each line, it is abundantly clear to one of ordinary skill in the art that there are devices comparing for each data line (transition detectors));

The combination of Halbert and Kim and Wong fails to explicitly teach of a clock cycle counter; a plurality of data transition counters, each configured to count the data transitions, and configured to be reset by the clock cycle counter.

However, Boggs teaches of a clock cycle counter (fig. 2; column 5, line 54-column 6, line 3);

a plurality of data transition counters, each configured to count the data transitions, and configured to be reset by the clock cycle counter (fig. 2; column 6, lines 22-32, 41-46);

The combination of Halbert, Kim and Wong and Boggs teaches of a logic block configured to signal when at least one of the plurality of data transition counters counts, during a time period defined by the clock cycle counter, a number of data transitions detected by the corresponding data transition detector that is less than the desired data transition density (Kim, fig. 1; paragraph 0020-0025; in the combination, the control

signal is generated upon the number of transitions being under the N/2 value after the timer period as determined in Boggs).

It would have been obvious to one of ordinary skill in the art having the teachings of Halbert, Kim, and Wong and Boggs at the time of the invention to include the counters of Boggs in the combination of Halbert, and Kim and Wong. Their motivation would have been to provide increased flexibility in the driver in the combination of Halbert and Kim, which also allows for monitoring of transitions on a longer scale for better overall efficiency.

21. With respect to claim 9, Boggs teaches of wherein the clock cycle counter and the plurality of data transition counters are programmable (fig. 2; column 5, lines 51-61; column 6, lines 15-32; as the counter (clock cycle counter) and the asynchronous counter (transition counter) are integrated circuits, it is abundantly clear to one of ordinary skill in the art that they are programmable).

22. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Halbert, Kim and Wong and Boggs as applied to claim 8 above, and further in view of the applicant's admitted prior art (AAPA).

23. With respect to claim 10, Halbert, Kim and Wong and Boggs fails to explicitly teach of wherein the logic block comprises an AND gate and a plurality of NAND gates.

However, AAPA teaches of wherein the logic block comprises an AND gate and a plurality of NAND gates (specification page 4, lines 18-21, 25-27).

It would have been obvious to one of ordinary skill in the art having the teachings of Halbert, Kim, Wong, Boggs and AAPA at the time of the invention to include the

NAND and AND gates of AAPA in the combination of Halbert, Kim, Wong, Boggs. Their motivation would have been to as those with ordinary skill in the art are familiar with using the NAND and AND gates to create output signals (AAPA, page 4, lines 19-21, 25-27) such as the control signal of Kim.

24. Claims 11-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Halbert and Kim and Wong as applied to claim 5 above, and further in view of Boggs and Little.

25. With respect to claim 11, the combination of Halbert, Kim, Wong, Boggs teaches of the limitations cited with respect to claim 8. Additionally, the combination teaches of the above first logic block with respect to data lanes on the outbound data path (Halbert, fig. 10-13; paragraphs 0053-0056, 0058; as the unidirectional components create an inbound and outbound path. Kim teaches of an output driver, which is applied to the output paths of the memory of the combination).

The combination of Halbert, Kim, Wong, Boggs, and Little teaches of a second logic block analogous to the first logic block from Kim, but is located in the CPU of Halbert on the output of the CPU, thus on the inbound data lines of the memory.

It would have been obvious to one of ordinary skill in the art having the teachings of Halbert, Kim, Wong, Boggs and Little at the time of the invention to include a data output driver of Kim in the CPU of Halbert, which is supported by Little. Their motivation would have been to reduce the skew of the output of data (Kim, paragraph 0009).

26. With respect to claim 12, Boggs teaches of the limitations as cited with respect to claim 9.

27. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Halbert, Kim, Wong, Boggs, and Little as applied to claim 11 above, and further in view of AAPA.

28. With respect to claim 13, AAPA teaches of the limitations as cited above with respect to claim 10.

It would have been obvious to one of ordinary skill in the art having the teachings of Halbert, Kim, Wong, Boggs, and Little and AAPA at the time of the invention to include the NAND and AND gates of AAPA in the combination of Halbert, Kim, Wong, Boggs and LIttle. Their motivation would have been to as those with ordinary skill in the art are familiar with using the NAND and AND gates to create output signals (AAPA, page 4, lines 19-21, 25-27) such as the control signal of Kim.

29. Claims 14-15 rejected under 35 U.S.C. 103(a) as being unpatentable over Halbert, Kim, Wong, Boggs et al., US patent 5530696, and Bliss et al., US patent application publication 2004/0056782.

30. With respect to claim 14, Halbert teaches of a data lane in a point-to-point memory channel (fig. 10-13; paragraph 0053-0056);

Kim teaches of storing a desired data transition number (paragraph 0020-0022; as the value of N/2 is used as the threshold, it is abundantly clear to one of ordinary skill in the art that the N/2 value is stored in order for it to be used in the comparison);

recording a measured data transition number (paragraph 0020; it is abundantly clear to one of ordinary skill in the art that as the number is used in a comparison that is has been stored);

comparing the measured data transition number to the desired data transition number (paragraph 0020-0022)

Boggs teaches of storing a clock cycle number (fig. 2; column 5, line 54-column 6, line 3; where the three counters count the clock transitions until 1024 transitions have been reached. As this number is used as the max to count to it is clear to one of ordinary skill in the art that it is in effect 'stored' in the counter);

recording a measured data transition number over a period of clock cycles equal to the clock cycle number (fig. 2; column 6, lines 22-32, 41-46);

Wong teaches of the clock cycle number being greater than two (abstract, column 2, lines 16-33, column 8, lines 49-52).

The combination of Halbert, Kim, and Boggs fails to explicitly teach of a machine-readable medium, that when read, causes a machine to perform processes. However, Bliss teaches of a machine-readable medium, that when read, causes a machine to perform processes (paragraph 0017).

It would have been obvious to one of ordinary skill in the art having the teachings of Halbert, Kim, Wong and Boggs at the time of the invention to include the counters of Boggs in the combination of Halbert, and Kim and Wong. Their motivation would have been to provide increased flexibility in the driver in the combination of Halbert and Kim and Wong, which also allows for monitoring of transitions on a longer scale for better efficiency.

It would have been obvious to one of ordinary skill in the art having the teachings of Halbert, Kim, Wong, Boggs, and Bliss at the time of the invention to incorporate the

processes and software carrying out the combination of Halbert, Kim Wong, and Boggs into the computer readable medium of Bliss. Their motivation would have been to provide for ease of upgrading and portability.

31. With respect to claim 15, Kim teaches of transmitting a synchronization signal on the data lane if the measured data transition number is less than the desired data transition number as cited above with respect to claims 1 and 5.

32. Claims 26, 27 rejected under 35 U.S.C. 103(a) as being unpatentable over Halbert, and Kim and Wong as applied to claim 5 above, in further view of Gray, 2002/0083286.

33. With respect to claim 26, the combination of Halbert and Kim and Wong teaches of the transition detection circuit is configured to detect whether an achieved data transition density on at least one data lane is less than the desired data transition density for the at least one data lane (Kim, fig. 1; item 104; paragraph 0018-0022).

Halbert and Kim and Wong fails to explicitly teach of the transition detection circuit detecting whether an achieved data transition density on a corresponding one of the at least one data lane is less than the desired data transition density for the corresponding lane.

However, Gray teaches of a transition detector for each data line (fig. 2; paragraph 0026).

It would have been obvious to one of ordinary skill in the art having the teachings of Halbert, Kim and Gray at the time of the invention to include multiple transition detectors, one for each line in the combination of Halbert and Kim, as taught in Gray.

Their motivation would have been to provide more flexibility and control over the data input/output process.

34. With respect to claim 27, the combination of Halbert, Kim, wong, and Gray teaches of wherein the corresponding data lane is a serial data lane (Kim, fig. 1; in the combination, each data lane (md0) only transmits one data part at a time; it is clear that it is a serial data lane).

Response to Arguments

35. Applicant's arguments filed 3/12/2007 have been fully considered but they are not persuasive.

36. The applicant argues with respect to the 35 U.S.C. 112 1st paragraph rejection for claim 27 that support for the data lanes being serial data lanes comes from where the specification says they are differential signals. The applicant argues that it is known that differential signals can be serial signals, thus the specification has support. The examiner disagrees. A differential signal is not required to be a serial signal in order to be a differential signal. Differential signals are also known to be parallel signals and stating that a signal is a serial differential signal is more specific than just saying a signal is a differential signal, what the applicant's spec says. The applicant's specification needed to have explicitly mentioned the signal being a serial signal for there to be support for such.

37. Applicant's arguments with respect to the independent claims have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

38. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

39. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael Krofcheck whose telephone number is 571-272-8193. The examiner can normally be reached on Monday - Friday.

40. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on 571-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

41. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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